

REMARKS

Claims 1, 6, 9, 10 and 14 are pending in the present application. Claims 1 and 9 have been amended.

Claim Rejections – 35 U.S.C. 103

Claims 1, 6, 9, 10 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Chiu et al. reference (U.S. Patent No. 4,514,897) in view of the Gardner et al. reference (U.S. Patent No. 5,888,870). This rejection is respectfully traversed for the following reasons.

The method of manufacturing a non-volatile semiconductor storage device of claim 1 includes in combination among other features “a first step of successively forming a first insulating film and a first polysilicon layer on a semiconductor substrate, and implanting nitrogen ions into a front surface of the first polysilicon layer”; “a second step of patterning a first polysilicon layer and a first insulating film into the shape of a band”; and “a third step of thermally oxidizing the patterned band-shaped first polysilicon layer, thereby to form a second insulating film which is thicker at side surfaces of the first polysilicon layer than at the front surface thereof”. Applicant respectfully submits that the method of manufacturing a nonvolatile semiconductor storage device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner.

As emphasized beginning on page 11 of the Amendment dated August 5, 2005, **and as reiterated in the Amendment dated August 15, 2006,** the Chiu et al. reference as relied upon by the Examiner does not specifically describe that silicon

dioxide layer 24 as shown in Fig. 2 is thicker at side surfaces of floating gate 13 than at a front surface of floating gate 13. As described in column 6, line 60-66 of the Chiu et al. reference with respect to Fig. 5d, silicon dioxide layer 24 is grown on the first level polysilicon, producing a coating on all exposed surfaces of the poly including tops and sides. Silicon dioxide layer 24 is grown at about 1100°C in O₂ for about 55 minutes and in N₂ for 30 minutes, "producing about 1200 Å thickness and consuming part of the polysilicon". There is no specific description pertaining to different respective silicon dioxide layer thicknesses.

In the Response to Arguments section on page 7 of the Final Office Action dated May 17, 2006, the Examiner asserted that:

"As shown in Fig. 2, the silicon oxide layer 24 appears thicker in bottom edge surface of the floating gate 13 than the top surface of floating gate 13. In addition, in the absence of specification thickness range of the silicon oxide layer on the top surface relative to the sidewall surface of the floating gate applicant's own drawings are not drawn to scale" (our emphasis added).

However, as asserted in the Amendment dated August 15, 2006, Applicant respectfully submits that in absence of specific description in the Chiu et al. reference that silicon dioxide layer 24 is thicker on side surfaces of poly 13 than on a front surface thereof, and/or in absence of any reasoning whatsoever as offered by the Examiner that would specifically establish why silicon dioxide layer 24 would be formed thicker on side surfaces of poly 13 in view of the processing parameters as set forth in the Chiu et

al. reference, **1) it must be considered that any perceived difference in thickness of silicon dioxide layer 24 in Figs. 2 and 7 of the Chiu et al. reference is merely incidental and an artifact of the drawing figure.** Particularly, silicon dioxide layer 24 of the Chiu et al. reference would appear to be substantively conformal.

THE EXAMINER HAS HOWEVER FAILED TO ANSWER THE SUBSTANCE OF THIS ABOVE INDICATED FIRST TRAVERSAL ON THE RECORD.

As asserted in the Amendment dated August 15, 2006, and as described beginning on page 7, line 9 of the specification of the present application with respect to Fig. 3A, nitrogen ions (N) are implanted into the front surface of polysilicon layer 14A. The implantation conditions of nitrogen ions are therein described. As further described beginning on page 8 of the present application, during the corresponding thermal oxidation, since the front surface of polysilicon layer 14B has been implanted with nitrogen ions, the growth of the oxide film is slower at the front surface of polysilicon layer 14B than at side surfaces thereof where no nitrogen ions exist. As subsequently described beginning on page 8, line 8 of the present application with respect to Fig. 3C, inter-gate insulating film 15a is therefore about 10nm thick on the front surface of polysilicon layer 14B, and inter-gate insulating film 15b is about 12-20nm thick on side surfaces of polysilicon layer 14B and tunnel oxide film 13.

Accordingly, contrary to the Examiner's assertion on page 7 of the Final Office Action, **2) thickness ranges of the silicon oxide layer on top and side surfaces of the polysilicon layer are described, and the thickness of inter-gate insulating layers 15a and 15b in Figs. 3A-3E of the present application may be perceived to be relatively to scale.**

**THE EXAMINER HAS HOWEVER FAILED TO ANSWER THE SUBSTANCE
OF THIS ABOVE INDICATED SECOND TRAVERSAL ON THE RECORD.**

As also noted in the Amendment dated August 15, 2006, the Examiner has further asserted on page 7 of the Final Office Action that "Limitations appearing in the specification but not recited in the claim are not read into the claim". Applicant respectfully submits that 3) this position as taken by the Examiner is improper and misrepresentative of the issues, because claim 1 clearly features "a third step of thermally oxidizing the patterned band-shaped first polysilicon layer, thereby to form a second insulating film which is thicker at side surfaces of the first polysilicon layer than at the front surface thereof".

**THE EXAMINER HAS HOWEVER FAILED TO ANSWER THE SUBSTANCE
OF THIS ABOVE INDICATED THIRD TRAVERSAL ON THE RECORD.** The Examiner is respectfully requested to clarify the above noted position on the record, or to withdraw the statement of record.

In summary for the record, Applicant respectfully submits that the Examiner has failed to directly address the above noted arguments in the current Office Action dated October 5, 2006. In particular, it is been asserted in the Amendment dated August 5, 2005 and in the Amendment dated August 15, 2006, that the Chiu et al. reference does not specifically describe that silicon dioxide layer 24 as shown in Fig. 2 is thicker at side surfaces of floating gate 13 than at a front surface of floating gate 13. Detailed arguments have been presented by the Applicant in support of this assertion. The Examiner has however refused to directly address these traversals, contrary to the guidelines as set forth in Manual of Patent Examining Procedure (MPEP) section

707.07(f). This despite Applicant's request to do so in the last paragraph on page 8 of the Amendment dated August 15, 2006. Applicant has thus been denied full and fair hearing, and the record with respect to this application is incomplete. Should this application proceed to appeal, the Board will not be put on notice as to whether the arguments have been considered, and why the arguments have been deemed unpersuasive.

With further regard to this rejection, the Examiner has acknowledged that the Chiu et al. reference does not specifically disclose implanting nitrogen ions into a front surface of the first polysilicon layer. In an effort to overcome this acknowledged deficiency, the Examiner has relied upon the Gardner et al. reference as described with respect to Figs. 3-5. Applicant however respectfully submits that the Gardner et al. reference as relied upon does not disclose or suggest a silicon dioxide layer formed on a floating gate, whereby the silicon dioxide layer is thicker at side surfaces of the floating gate than at a front surface of the floating gate, as would be necessary to overcome the above noted deficiencies of the primarily relied upon Chiu et al. reference.

Applicant therefore respectfully submits that the method of manufacturing a nonvolatile semiconductor storage device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1 and 6 is improper for at least these reasons. **The Examiner is respectfully requested to take note of the traversals initially presented in the Amendment dated August 5, 2005, and subsequently reiterated in the Amendment dated August 15, 2006, and to answer the substance of the**

traversals on the record.

The method of manufacturing a semiconductor device of claim 9 features in combination among other features “implanting nitrogen ions into a front surface of the first polysilicon layer”; “thermally oxidizing the band-shaped segment to simultaneously grow the second insulating film on side surfaces and the front surface of the first polysilicon layer, wherein the second insulating film is grown thicker on the side surfaces of the first polysilicon layer than on the front surface of the polysilicon layer implanted with nitrogen ions;...wherein said implanting nitrogen ions is performed prior to said patterning the first insulating film”.

Applicant respectfully submits that the primarily relied upon Chiu et al. reference does not disclose a second insulating film that is thicker on side surfaces of a first polysilicon layer than on a front surface of a polysilicon layer implanted with nitrogen ions. The secondarily relied upon Gardner et al. reference also fails to disclose these above noted features. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 9, 10 and 14, is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

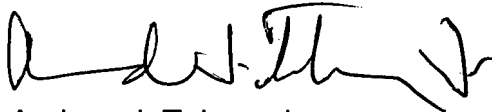
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to April 5, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of \$1020.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.

A handwritten signature in black ink, appearing to read 'Andrew J. Telesz, Jr.', with a stylized flourish at the end.

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